

What is Claimed is:

1. A semiconductor chip having a semiconductor substrate, a first external electrode formed on a first surface of said semiconductor substrate, a second external electrode formed on a second surface of said semiconductor substrate and a through hole created in said semiconductor substrate, wherein the semiconductor chip is characterized in that said through hole is created in an inclined plane formed so that the inner angle made up of said second surface and the inclined surface is an obtuse angle and that said first external electrode and said second external electrode are electrically connected through a conductive pattern which is formed so as to follow the inner walls of said through hole and said inclined surface.

2. A semiconductor chip having a semiconductor substrate, a surface electrode formed on a first surface of said semiconductor substrate and a thorough hole created in said semiconductor substrate, wherein said through hole is created in an inclined plane formed so that the inner angle made up of a second surface and the inclined surface is an obtuse angle and wherein the semiconductor chip is characterized by comprising a first insulating layer formed on said first surface except for on said surface electrode, on the inner walls of said through hole, on said inclined plane and on said second surface, a conductive pattern which is filled into said through hole and which is formed on said first insulating layer and on said surface electrode

and a second insulating layer formed with an opening for a part of the surface of said conductive pattern on said first surface as a first external electrode and with an opening for a part of the surface of said conductive pattern on said second surface as a second external electrode.

3. A semiconductor chip comprising a semiconductor substrate which has a top surface on which elements are integrally formed, a rear surface which opposes to said top surface in a parallel manner, an inclined plane formed so that said top surface and the inclined plane form an acute angle and a recess which is created around said top surface and which continues to said inclined plane, wherein the semiconductor chip comprises a first electrode formed on said top surface, a second electrode formed on said rear surface and a conductive pattern which is formed within said recess and on said inclined plane and which is for connecting said first electrode and said second electrode.

4. A semiconductor chip comprising a semiconductor substrate which has a top surface on which elements are integrally formed, a rear surface which opposes to said top surface in a parallel manner, an inclined plane formed so that said top surface and the inclined plane form an acute angle and a recess which is created around said top surface and which continues to said inclined plane and has a surface electrode which is connected to said elements, wherein the semiconductor chip comprises a first insulating layer formed on the inside walls of said recess

and on said top surface other than on said surface electrode, a first conductive pattern which is filled into said recess where said first insulating layer is formed and which is formed on said top surface where said first insulating layer is formed in a desired wire and electrode form so as to be connected to said surface electrode, a second insulating layer formed on said top surface with openings for an electrode part made of said first conductive pattern, an inclined part where said first conductive pattern in said recess is exposed so as to continue to said inclined plane around said rear surface, a third insulating layer formed on said rear surface and on said inclined plane with an opening for said inclined part from which said first conductive pattern is exposed, a second conductive pattern which is formed on said inclined plane where said third insulating layer is formed and on the rear surface of said semiconductor chip in a desired wire and electrode form so as to be connected to said first conductive pattern and a fourth insulating layer formed on the rear surface and on said inclined plane of said semiconductor chip with an opening for an electrode part made of said second conductive pattern.

5. A semiconductor chip according to Claim 2 or 4, wherein a layered metal film is formed between the first insulating layer and the conductive pattern as well as between the surface electrode and the conductive pattern.

6. A semiconductor chip according to Claim 2, 4 or 5, wherein

the conductive patterns, except for at least one, are formed in the surface electrode.

7. A semiconductor chip according to Claim 2 or 4, wherein a vertical side surface is formed of an insulating resin supplied to the inclined plane.

8. A semiconductor chip according to Claim 5, wherein the layered metal film comprises a barrier layer and a seed layer.

9. A wiring board of which the base material is silicon, characterized in that a plurality of through holes are created in said wiring board, a first conductive pattern is formed on a surface of said wiring board, said through holes are created in an inclined plane formed so that the inner angle made up of the a rear surface of said wiring board and the inclined plane is an obtuse angle, a second conductive pattern is formed on said rear surface and on said inclined plane and said first conductive pattern and said second conductive pattern are electrically connected through a third conductive pattern formed in said plurality of through holes.

10. A wiring board for a multi-chip semiconductor device on which electronic parts are mounted and which is mounted on a mother board, characterized in that said wiring board has a silicon substrate made of silicon, in that a first conductive pattern for mounting and wiring said electronic parts which is made of, at least, one layer is provided on a top surface of this silicon substrate and a second conductive pattern made of,

at least, one layer which has an electrode for being mounted on said mother board is provided on a rear surface of said silicon substrate and in that said first conductive pattern and said second conductive pattern are electrically connected through a third conductive pattern formed on a side surface of said silicon substrate.

11. A wiring board for a multi-chip semiconductor device on which electronic parts are mounted and which is mounted on a mother board, wherein said wiring board is characterized by comprising a silicon substrate made of silicon wherein a side surface is formed so that a top surface and the side surface of the substrate form an acute angle while a recess is formed around the substrate, a first conductive pattern made of, at least, one layer having an electrode formed on the surface and within said recess of said silicon substrate and a second conductive pattern made of, at least, one layer having an electrode which is formed on the rear surface and on said side surface of said silicon substrate and which is connected to said first conductive pattern.

12. A wiring board according to Claim 9 or 11, wherein an insulating layer is formed on a side surface so that the surface of the insulating layer and the surface of the substrate form a right angle.

13. A wiring board according to Claim 9, 10 or 11, comprising a resin layer of low stress inserted either between the first

conductive pattern and the substrate or between the second conductive pattern and the substrate or inserted in both cases.

14. A process for a semiconductor chip characterized by comprising: the step of preparing a semiconductor substrate; the step of forming holes in peripheral parts of semiconductor chip units in said semiconductor substrate; the step of forming first external electrodes on a first surface of said semiconductor substrate and of forming first conductive patterns in said holes and on said first surface so as to be electrically connected to said first external electrodes; the step of forming inclined planes so that internal angles made up of the inclined planes and a second surface of said semiconductor substrate are obtuse angles and of allowing said holes to penetrate; and the step of forming second external electrodes on said second surface and of forming second conductive patterns on said inclined planes and on said second surface so as to electrically connect said second external electrodes and said first conductive patterns.

15. A process for a semiconductor chip characterized by comprising: the step of preparing a semiconductor substrate; the step of creating holes in peripheral parts of semiconductor chip units in said semiconductor substrate; the step of forming a first insulating layer on a first surface, except for on a surface electrode, and on inner walls of said holes of said semiconductor substrate; the step of forming first conductive patterns on said first insulating layer and filling the first

conductive patterns into said holes; the step of forming a second insulating layer with openings for parts of a surface of said first conductive patterns as first external electrodes; the step of polishing a second surface so that said semiconductor substrate becomes of a desired thickness; the step of forming inclined planes wherein internal angles made up of the inclined planes and said second surface are obtuse angles in the border parts between said semiconductor chip units in said second surface and, at the same time, of allowing said holes to penetrate to said inclined planes; the step of forming a third insulating layer on said inclined planes except for said holes and on said second surface; and the step of forming second conductive patterns on said third insulating layer so as to be electrically connected to said first conductive patterns and the step of forming a fourth insulating layer with openings for parts of a surface of said second conductive patterns as second external electrodes.

16. A process for a plurality of semiconductor chips gained from a wafer which has a top surface on which elements are integrally formed and a rear surface which is opposed to said top surface in a parallel manner, comprising: the step of creating a recess around said semiconductor chips in said top surface; the step of forming inclined planes in the semiconductor substrate so that said top surface and the inclined planes form acute angles; the step of forming first external electrodes on

said top surface; the step of forming second external electrodes on said rear surface; the step of forming first conductive patterns within said recess and said top surface so as to be connected to said first external electrodes and the step of forming second conductive patterns on said inclined planes and on said rear surface for connecting said second external electrodes and said first conductive patterns.

17. A process for a plurality of semiconductor chips gained from a wafer which has a top surface on which elements are integrally formed and a rear surface which is opposed to said top surface in a parallel manner, comprising: the step of creating recesses around said semiconductor chips along scribe lines on said top surface of said wafer so as to cross said scribe lines; the step of forming a first insulating layer on the inner walls of said recesses and on said top surface, except for on surface electrodes of said semiconductor chips; the step of forming first conductive patterns which are filled into said recesses wherein said first insulating layer is formed and which are formed on said top surface on which said first insulating layer is formed in desired wire and electrode forms; the step of forming a second insulating layer on said top surface with openings for electrode parts made of said first conductive patterns; the step of polishing said wafer starting from said rear surface so as to have a desired thickness; the step of forming inclined planes around rear surfaces of said semiconductor chips by cutting said



wafer along said scribe lines on said rear surface so that the inclined planes and the top surface form acute angles and, at the same time, of exposing said first conductive patterns within said recesses from said inclined planes; the step of forming a third insulating layer with openings for exposed parts of said first conductive patterns on said rear surface and on said inclined planes; the step of forming second conductive patterns on said inclined planes on which said third insulating layer is formed and on the rear surface of said semiconductor chips in desired wire and electrode forms so as to be connected to said first conductive patterns exposed from said inclined planes; and the step of forming a fourth insulating layer on said rear surface of said semiconductor chips and on said inclined planes with openings for electrode parts made of said second conductive patterns.

18. A process for a plurality of semiconductor chips according to Claim 14 or 16, wherein the step of forming the first external electrodes and the step of forming the first conductive patterns are carried out simultaneously.

19. A process for a plurality of semiconductor chips according to Claim 14 or 16, wherein the step of forming the second external electrodes and the step of forming the second conductive patterns are carried out simultaneously.

20. A process for a plurality of semiconductor chips according to Claim 15 or 17, characterized by providing the step of forming

a first layered metal film on said first insulating layer between the step of forming a first insulating layer and the step of forming first conductive patterns while providing the step of forming a second layered metal film on said third insulating layer between the step of forming a third insulating layer and the step of forming second conductive patterns.

21. A process for a plurality of semiconductor chips according to Claim 15, 17 or 20, wherein the fourth insulating layer is formed by applying and curing a liquid resin and by division into semiconductor chip pieces is carried out through dicing.

22. A process for a plurality of semiconductor chips according to Claim 15 or 17, characterized in that the step of forming inclined planes at the edges of said second surface wherein internal angles made up of the second surface and the inclined planes are obtuse angles is carried out through bevel cutting on said second surface.

23. A process for a plurality of semiconductor chips according to Claim 15, 17 or 20, characterized in that the rate of etching of the third insulating layer is greater than the rate of the etching of the first insulating layer or of the second insulating layer.

24. A process for a plurality of semiconductor chips according to Claim 17, wherein said recesses are trenches created by means of dicing.

25. A process for a wiring board characterized by comprising:

the step of creating holes in the top surface of a silicon substrate; the step of forming a first conductive pattern on said top surface and in said holes; the step of forming inclined planes in a region confining a border part between substrate piece units on the rear surface so that internal angles made up of the rear surface of said silicon substrate and the inclined planes are obtuse angles and, at the same time, of exposing said first conductive patterns by allowing said holes to penetrate; and the step of forming second conductive patterns electrically connected to said first conductive patterns on said rear surface and on said inclined planes.

26. A process for a wiring board for a multi-chip semiconductor device, comprising: the step of forming first conductive patterns made of, at least, one layer for mounting and wiring electronic parts on a top surface of a silicon wafer; the step of forming second conductive patterns made of, at least, one layer having electrodes for being mounted to a mother board on a rear surface of said silicon wafer; the step of forming side surfaces by dividing said silicon wafer into silicon substrate pieces and the step of forming third conductive patterns for electrically connecting said first conductive patterns and said second conductive patterns on said side surfaces, wherein the process for a wiring board for a multi-chip semiconductor device is characterized in that the step of forming side surfaces by dividing the silicon wafer into silicon substrate pieces is

carried out after the step of forming first conductive patterns and, after that, the step of forming second conductive patterns and the step of forming third conductive patterns are carried out simultaneously.

27. A process for a wiring board for a multi-chip semiconductor device, comprising: the step of creating a recess around a top surface of a silicon substrate in a wafer condition; the step of forming a first conductive pattern made of, at least, one layer having an electrode on said top surface and within said recess; and the step of forming an inclined plane in said silicon substrate so that said top surface and the inclined plane form an acute angle and the step of forming a second conductive pattern, which is electrically connected to the first conductive pattern and which is made of, at least, one layer having an electrode, on a rear surface of said silicon substrate and on said inclined plane.

28. A process for a wiring board for a multi-chip semiconductor device according to Claim 25 or 27, characterized by including the step of forming an insulating layer on the inclined plane so that the top surface of the silicon substrate and the surface of the insulating layer form a right angle, wherein said insulating layer is formed by applying and curing a liquid resin and is divided into pieces through dicing.

29. A process for a wiring board for a multi-chip semiconductor device according to Claim 25 or 27, characterized by providing

the step of forming a resin layer of low stress between the substrate and the first conductive pattern or between the substrate and the second conductive pattern.

30. A semiconductor device, characterized in that a plurality of semiconductor chips, comprising semiconductor substrates, first external electrodes formed on first surfaces of said semiconductor substrates, second external electrodes formed on second surfaces of said semiconductor substrates and through holes created in said semiconductor substrates, wherein said through holes are created in inclined planes formed so that the internal angles made up of said second surfaces and the inclined planes are obtuse angles and said first external electrodes and said second external electrodes are electrically connected through conductive patterns formed so as to follow the inner walls of said through holes and said inclined planes, are layered while said respective first external electrodes and said respective second external electrodes are electrically connected.

31. A semiconductor device characterized in that between two first semiconductor chips comprising semiconductor substrates, first external electrodes formed on first surfaces of said semiconductor substrates, second external electrodes formed on second surfaces of said semiconductor substrates and through holes created in said semiconductor substrates, wherein said through holes are created in inclined planes formed so that the

internal angles made up of said second surfaces and the inclined planes are obtuse angles and said first external electrodes and said second external electrodes are electrically connected through first conductive patterns formed so as to follow the inner walls of said through holes and said inclined planes, a second semiconductor chip wherein third external electrodes formed in the parts other than the region of the third surface on which elements are formed and fourth external electrodes formed in the parts other than the region of the fourth surface on which elements are formed are electrically connected through second conductive patterns is provided so that said first semiconductor chips and said second semiconductor chip are electrically connected directly or via connection members.

32. A multi-chip type semiconductor device formed by layering a plurality of semiconductor chips comprising semiconductor substrates with top surfaces on which elements are integrally formed, wherein said layered semiconductor chips comprise semiconductor substrates having said top surfaces, rear surfaces which are opposed to said top surfaces in a parallel manner, inclined planes formed so that the inclined planes and said top surfaces form acute angles and recesses created in the periphery around said top surfaces and comprise first external electrodes formed on said top surfaces, second external electrodes formed on said rear surfaces and conductive patterns formed in said recesses and on said side surfaces for connecting said first

external electrodes and said second external electrodes and wherein said semiconductor chips are electrically connected to other semiconductor chips via said first external electrodes and said second external electrodes.

33. A semiconductor device according to Claim 32, wherein the layered semiconductor chips are electrically connected to other semiconductor chips directly above and directly below said semiconductor chips by directly connecting the electrodes thereof or via connection members.